Tau™ 2 Electrical Interface Description Document (IDD)

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1 Document

1.1 Revision History

Version	Date	Comments
100	11/07/2011	Initial Release
110	08/01/2012	Modified to reflect Tau 2.1 interface. Specifically, the following is changed: • 3.1.2: Slight increase in power consumption (result of larger feature set / higher processing load of Tau 2.1) • 3.1.6.1: Master-mode external-sync pulse width increased from 100 nsec to 1 usec. Other changes: • 2.1, 2.4: Added FLIR Website / Contact info and Glossary of Acronyms
120	12/20/2012	Modified to reflect Tau 2.2 interface. Specifically, the following is changed: • 3.1.1, 3.1.4.1: Noted that BT.656 is not available in Tau 2.2 • 3.1.4.2: Made notes on 8-bit CMOS frame rate and behavior during FFC
130	06/06/2013	Modified to reflect Tau 2.4 interface. Specifically, the following is changed: • 3.1.4.2 and 3.1.4.3: Updated 8-bit CMOS and LVDS field-selectable options, frame rate, and FFC operation with Tau 2.4 "Digital eZoom Mode" • 3.1.4.3: Added that symbol overlay is not applicable for 8-bit mode, updated LVDS timing descriptions for updated to Figure 5 • Updated Table 4 and added Table 5 to include Tau 2.4 power dissipation • Updated Table 7 to depict frame rates for Tau 2.4 "Digital eZoom Mode" and added Note 4 • Updated Figure 3 and Figure 4 to include the 160, 324, 336, and 640 configs • Updated Figure 5 for correct LVDS timing and included 160, 324, 336, and 640 configs
131	10/22/2013	• Corrected Table 2 to have EXT_SYNC as input or output • 3.1.6.2 Noted that FLIR does not recommend slave mode for analog video
140	05/19/14	Modified to reflect Tau 2.7 interface. Specifically, the following has changed and is highlighted in blue text throughout the document: • 3.1.4.1 Removed BT.656 note about only digital output with color/symbols • 3.1.4.2 Updated CMOS digital output options and clock rate for 640, 60Hz option • 3.1.4.3 Updated LVDS digital output options and clock rate for 640, 60Hz option • 3.1.6 Updated External Sync behavior • Updated Table 1 to redefine pin 40 from "reserved" to "XP1_CLK2". Changed pin 39 from "XP1_CLKOUT" to "XP1_CLK1". • Updated Table 2 to include new 16-bit CMOS pin assignments. Note that this mode utilizes pin 40, which was currently unused in any of the XP1 modes. Therefore, pin 40 is added to the table. • Updated Table 7: Included 640, 60Hz option General updates: • 3.1.2 Added statement about power interruption during flash operations. • 3.1.7 Clarified voltage: OK to apply more than 3.3 V to serial input.
141	06/16/14	• 3.1.4.2 Update CMOS clock rates, added details about clock for 8-bit double clocked mode • Added Table 6 for Power Consumption

		• Table 8, added Note 5 to define resolution changes with "digital eZoom mode" • Figure 3: updated original figure and added (b) and (c) to show line timing for YCbCr modes • Table 9: Added frequency ranges for Slave mode

1.2 Scope

Tau ™ is a miniature infrared imaging core from FLIR Systems®. This Interface Description Document (IDD) defines electrical interface requirements for the Tau 2 configuration of the product.

Note: A number of expansion cards intended for specific applications are available for Tau. In most cases, these expansion cards modify or augment the standard core interfaces. This IDD only applies to the standalone core.

2 References

The following documents form a part of this specification to the extent specified herein.

2.1 FLIR Website / Contact Information

In multiple locations throughout this document, FLIR's Tau / Quark website is referenced as a source of additional information. This websites can be accessed via the following URL:

www.flir.com/cvs/cores/uncooled/products/tau/

http://www.flir.com/cvs/cores/uncooled/products/quark/

Additionally, FLIR's Applications Engineering Department is referenced as a resource for obtaining additional help or information. The department can be accessed via the following phone number: +1-805-964-9797 (or toll-free within the United States at 888-747-FLIR (888-747-3547).) Email requests can be addressed to SBA-cores@flir.com.

2.2 FLIR Systems Documents

102-PS242-40	Tau 2 Product Specification
102-PS242-43	Tau 2 / Quark Software Interface Description Document

2.3 External Documents

ANSI/TIA/EIA-232 (formerly RS232)	Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange
ANSI/TIA/EIA-644	Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
EIA-170A	Composite Analog Video Signal – NTSC for Studio Applications
ITU Rec. BT.656	Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601

2.4 Acronyms / Abbreviations

AGC	Automatic Gain Control
CMOS	Complementary Metal Oxide Semiconductor
FFC	Flat Field Correction
FPA	Focal Plane Array
IDD	Interface Description Drawing / Document
LVDS	Low-Voltage Differential Signaling
NTSC	National Television System Committee
PAL	Phase Alternating Line
RX	Receive
TX	Transmit
XP	eXPansion

3 Electrical Interface Requirements

This document defines requirements for the following Tau 2 interfaces:

- Power
  - Input power
  - 3.3V output
- Analog video data
- Digital video data
  - Parallel channel (single-ended)
  - Serial channel (LVDS)
- Discrete I/O (user-configurable)
- Frame-sync interface (optional)
- Communication interface

3.1.1 Interface Connector

a. The electrical interface to the Tau 2 core is via a single high-density 50-pin connector: Hirose #DF12-50DS-0.5V(86). The recommended mating connector is Hirose #DF12(5.0)-50DP-0.5V(86) for a mating stack height of 5mm.

b. Pin definitions are shown in Table 1. See Figure 1 for a picture showing the pin numbering of the connector. The pin-out is backwards-compatible with Tau 1.X configurations. In other words, a Tau 2.X can be plugged into the same socket as a Tau 1.X core and will generally operate identically with one exception: for all Tau 2 configurations, the LVDS protocol employs two data lines (see 3.1.4.3) whereas for Tau 1.5 (324x256 configuration), the LVDS protocol employed a single data line.

c. The pins defined as “XP” in Table 1 are reconfigurable by the user. Table 2 shows the pin assignments of the XP bus as a function of selected XP mode.

Table 1: Primary I/O Connector Pin Definition

Pin #	Signal Name	Pin #	Signal Name
1	RS232_TX (see 3.1.7)	2	RS232_RX (see 3.1.7)
3	XP_D17	4	XP_D16
5	DGND	6	DGND
7	Reserved	8	Reserved
9	LVDS_CLK_P (see 3.1.4.3)	10	LVDS_CLK_N (see 3.1.4.3)
11	LVDS_SYNC_P (see 3.1.4.3)	12	LVDS_SYNC_N (see 3.1.4.3)
13	LVDS_DATA1_P (see 3.1.4.3)	14	LVDS_DATA1_N (see 3.1.4.3)
15	LVDS_DATA2_P (see 3.1.4.3)	16	LVDS_DATA2_N (see 3.1.4.3)
17	DGND	18	DGND
19	XP_D15	20	XP_D14
21	XP_D13	22	XP_D12
23	XP_D11	24	XP_D10
25	XP_D9	26	XP_D8
27	DGND	28	DGND
29	XP_D7	30	XPD_6
31	XP_D5	32	XPD_4
33	XP_D3	34	XPD_2
35	XP_D1	36	XPD_0
37	DGND	38	DGND
39	XP_CLK1	40	XP_CLK2
41	DGND	42	DGND
43	VIDEO_H (see 3.1.3)	44	VIDEO_L (see 3.1.3)
45	DGND	46	3V3_OUT (see 3.1.2)
47	MAIN_PWR_RTN (see 3.1.2)	48	MAIN_PWR (see 3.1.2)
49	MAIN_PWR_RTN (see 3.1.2)	50	MAIN_PWR (see 3.1.2)

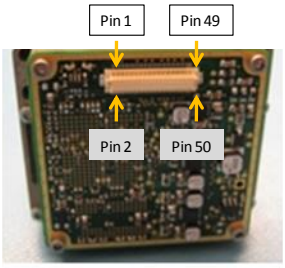


Figure 1: Primary I/O Connector Pinout, Hirose #DF12-50DS-0.5V(86)

Table 2: XP Bus Reconfigurable Pins

XP1 Bus Signal	Pin #		XP1 Mode (Field-Selectable)			
		BT.656 (see 0)	CMOS 16-bit	CMOS 14-bit (see 3.1.4.2)	CMOS 8-bit (see 3.1.4.2)	Data Disabled
XP_CLK1	39	BT656_CLK	CMOS_CLK	CMOS_CLK	CMOS_CLK	z
XP_CLK2	40	z	EXT_SYNC	z	Z	z
XP_D0	36	BT656_D0	CMOS_D0	CMOS_D0	CMOS_D0	z
XP_D1	35	BT656_D1	CMOS_D1	CMOS_D1	CMOS_D1	z
XP_D2	34	BT656_D2	CMOS_D2	CMOS_D2	CMOS_D2	z
XP_D3	33	BT656_D3	CMOS_D3	CMOS_D3	CMOS_D3	z
XP_D4	32	BT656_D4	CMOS_D4	CMOS_D4	CMOS_D4	z
XP_D5	31	BT656_D5	CMOS_D5	CMOS_D5	CMOS_D5	z
XP_D6	30	BT656_D6	CMOS_D6	CMOS_D6	CMOS_D6	z
XP_D7	29	BT656_D7	CMOS_D7	CMOS_D7	CMOS_D7	z
XP_D8	26	DISCRETE5	CMOS_D8	CMOS_D8	DISCRETE5	DISCRETE5
XP_D9	25	DISCRETE4	CMOS_D9	CMOS_D9	DISCRETE4	DISCRETE4
XP_D10	24	DISCRETE3	CMOS_D10	CMOS_D10	DISCRETE3	DISCRETE3
XP_D11	23	DISCRETE2	CMOS_D11	CMOS_D11	DISCRETE2	DISCRETE2
XP_D12	22	z	CMOS_D12	CMOS_D12	Z	z
XP_D13	21	EXT_SYNC	CMOS_D14	EXT_SYNC	EXT_SYNC	EXT_SYNC
XP_D14	20	DISCRETE1	CMOS_D13	CMOS_D13	DISCRETE1	DISCRETE1
XP_D15	19	DISCRETE0	CMOS_D15	DISCRETE0	DISCRETE0	DISCRETE0
XP_D16	4	DISCRETE_7	CMOS_FRAME_VALID	CMOS_FRAME_VALID	CMOS_FRAME_VALID	DISCRETE7
XP_D17	3	DISCRETE_6	CMOS_LINE_VALID	CMOS_LINE_VALID	CMOS_LINE_VALID	DISCRETE_6

Note: Purple font = output signal. Blue font = Input or Output. z = high impedance

Note: Tau 2.2 does not include the BT.656 digital output

3.1.2 Power Interface

a. The Tau 2 core provides full functionality when voltage as specified in Table 3 is applied across MAIN_PWR and MAIN_PWR_RTN.

b. For input voltage between the minimum value and the shutdown value specified in Table 3, core behavior is undefined. The Tau 2 core may reset continuously or may power down.

c. Certain user commanded operations such as saving settings to flash, erasing stored snapshots, or updating firmware require power to be provided for the duration of the operation. The interruption of power during a flash operation may leave the camera in an unusable state.

Note: The core does not provide internal protection against reverse-voltage or over-voltage.

Table 3: Tau 2 Input Power Requirements

Parameter	Value	Notes
Maximum voltage	6.0V	*Voltage in excess of this value may cause permanent damage to the core.*
Minimum voltage	4.0V or 4.4V	*The 4.0V requirement applies to the shutterless and standard shutter configs. The 4.4V requirement applies to the iris-style shutter configs.*
Shutdown voltage	0.0V - 3.8V	*See item b above.*
Average Power Dissipation	See Table 4, 5, and 6 below	*Varies by configuration and varies over temperature*
Surge current at start-up	< 600 mA	*Duration < 8 msec*
Max. current after start-up (during shutter cycle)	< 450 mA	

Table 4: Tau 2 Power Dissipation (Tau 2.1 Release)

Tau 2 Configuration	Power at 25C
324 / 336	≤ 1.10W
640	≤ 1.25W

Table 5: Tau 2 Power Dissipation (Tau 2.4 Release)

Tau 2 Configuration	Power at 25C
324 / 336	≤ 1.05W
640	≤ 1.20W

Table 6: Tau 2 Power Dissipation (Tau 2.7 Release)

Tau 2 Configuration	Power at 25C
324 / 336	≤ 0.99W
640	≤ 1.15W

Note: The values above assume a single digital channel (BT.656, CMOS, or LVDS) is enabled and that the analog channel is disabled. The values are increased by approximately 75 mW by disabling all digital channels and instead enabling analog.

d. The Tau 2 core provides an output voltage with characteristics as specified in Table 7 between the 3V3_OUT and DGND pins. This voltage is intended primarily for powering expansion electronics designed by FLIR Systems but may be applicable for other use.

Note: Loading down this voltage in excess of the peak supply current specified in Table 7 may cause the core to reset or behave unpredictably.

Table 7: 3V3 Characteristics

Parameter	Value
Voltage range	3.3V ± 3%
Peak supply current	100 mA

3.1.3 Analog Video Channel

a. The Tau 2 core provides analog video on the signals named VIDEO_H and VIDEO_L. Figure 2 shows required termination of the analog video channel. For transmission of the video channel, a coaxial cable with 75 ohm characteristic impedance is required.

b. The timing and voltage level of the analog video signal complies with either NTSC or PAL protocol. The choice between NTSC and PAL is field-selectable (via the serial comm. interface).

c. The channel may be disabled for a savings of approximately 75 mW.

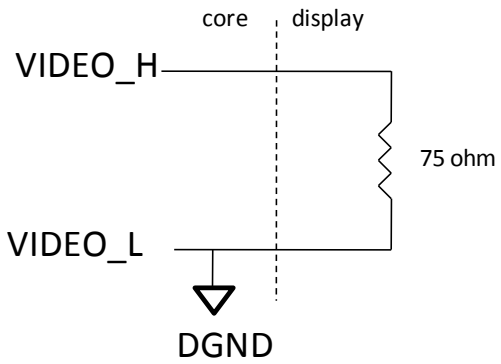


Figure 2: Required Termination of the Analog Channel

3.1.4 Digital Data Channels

a. The Tau 2 core provides the option of two simultaneous digital output channels, one parallel and one serial.

b. One or both channels can be disabled for a power savings of approximately 10 mW per channel.

c. The parallel channel can be field-configured to provide data via BT.656 protocol or a CMOS protocol, defined further in 3.1.4.1 and 3.1.4.2, respectively. Maximum recommended transmission length is approximately 1 m.

Note: BT.656 is not available in the Tau 2.2 release.

d. The serial port employs an LVDS protocol further defined in 3.1.4.3. Maximum recommended transmission length is approximately 3 m.

Note: Because the BT.656 and CMOS output are provided on a reconfigurable XP Bus available to multiple interface types / data rates, external signal filtering is required to minimize radiated emissions. For a specific XP-bus configuration and customer application, signal and power filtering should be tailored when targeting a given EMI specification. It is recommended that filtering be located immediately after the Tau mating connector. The filter type should address the extended harmonic frequencies of the XP Bus signaling and not cripple the signal shape and timing. The filter could be in the form of a series resistor or ferrite bead. The Tau chassis provides a flat metallic surface and four (4) mounting screw locations to fasten a mating PCB or Flex PCB. This surrounding chassis-attachment concept is the same as a cable shield.

3.1.4.1 BT.656 Protocol

The Tau 2 core provides the option of configuring the XP bus to output digital data with timing/format in compliance with ITU Recommendation BT.656.

Note: This interface is fully compliant with the Recommendation except in terms of line driver characteristics, ECL-compatibility, and connector type.

Note: This data channel is not available for the Tau 2.2 release.

1. The channel consists of a clock and 8 parallel bits of data, transmitted via single-ended 3.3V CMOS logic levels. See Table 2 for pin assignments.
2. The channel can only be configured for 8-bit (post-AGC) data. Symbol overlay and colorization are included in this output.
3. Clock frequency is 27 MHz. Refer to the ITU Recommendation for detailed timing / format requirements.
4. Frame rate is 29.97 Hz (NTSC) or 25.00 Hz (PAL). For “fast” 324 and 336 configurations, each data field is duplicated once (i.e., 2 fields per frame) whenever the averager feature is enabled. (See the Tau 2 Product Specification for more information on fast and slow configurations and the averager feature.) For the fast 640 configurations and for the fast 324 / 336 configurations with the averager disabled, each BT.656 field contains unique data.
5. For “slow” configurations, each data field is duplicated multiple times to produce an *effective* frame rate $\leq$ 9Hz.

3.1.4.2 CMOS Protocol

The Tau 2 core provides the option of configuring the XP bus to output a digital data protocol resembling that of a typical CMOS camera. Specifically:

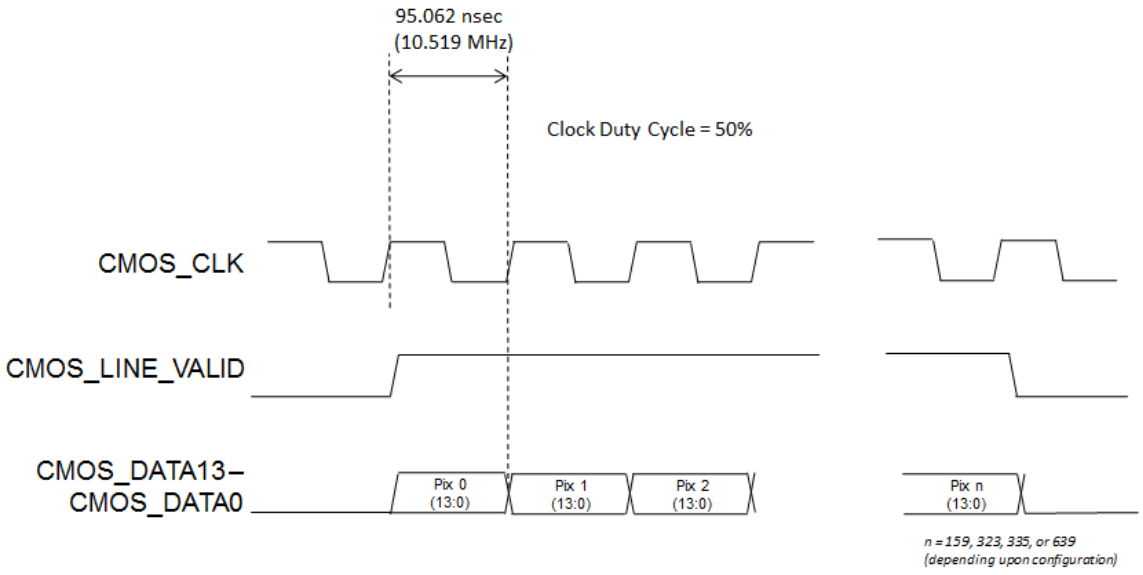
1. The channel consists of a clock, up to 14 parallel bits of data, a line-valid signal, and a frame-valid signal. The channel utilizes 3.3V CMOS logic levels. See Table 2 for pin assignments.
2. The choice between 14-bit (pre-AGC), 8-bit (post-AGC), 8-bit Bayer colorized, 16-bit YCbCr, and 8-bit double-clocked YCbCr data is field-selectable.
3. The field-selectable choice between 8-bit data with or without the continuous electronic zoom capability is also available. The "digital eZoom Mode" affects frame rate, resolution, and flat-field correction (refer to the Tau 2 Product Specification for further details). In the 8-bit digital eZoom mode with colorization enabled (via the Bayer or YCbCr modes) the user also has the option to enable symbology in the 8-bit channel.
4. Line timing is depicted in Figure 3. The clock rate is 21.04MHz for the 640, 60Hz configuration. The clock rate is 10.519MHz for all other configurations (e.g. 640 30Hz, 336, 324, and 160). The clock for the 8-bit YCbCr mode is doubled such that the clock rate is as follows: 42.08MHz for the 640, 60Hz configuration and 21.04MHz for the 640, 30Hz and 336 configurations.
5. The Bayer and YCbCr colorization modes are both user configurable. The Bayer encoding order is user-selectable. The YCbCr order is configurable for the 8-bit double-clocked mode ('YCbYCr' or 'CbYCrY'), and the sub-sampling is configurable for both 16-bit and 8-bit double-clocked modes ('4:2:2 centered' or '4:2:2 cosited'). See the Tau 2 Product Specification for further details. Figure 3b and Figure 3c shows the line timing for the 8-bit double clocked YCbCr mode and 16-bit YCbCr respectively ('YCbYCr' order, 4:2:2 cosited sub-sampling).
6. Frame timing is depicted in Figure 4. The frame rate depends upon configuration and settings as shown in Table 8.
7. No data is output on the CMOS channel during each flat-field correction (FFC) period. That is, LINE_VALID, DATA_VALID, and CMOS_DATA[0-13] are all disabled throughout FFC. While the "digital eZoom Mode" is enabled, the 8-bit data output continues during FFC. That is, the last frame before FFC is replicated during each FFC period. This mode does not affect the 14-bit data output.

Table 8: Frame Rate vs. Configuration / Settings

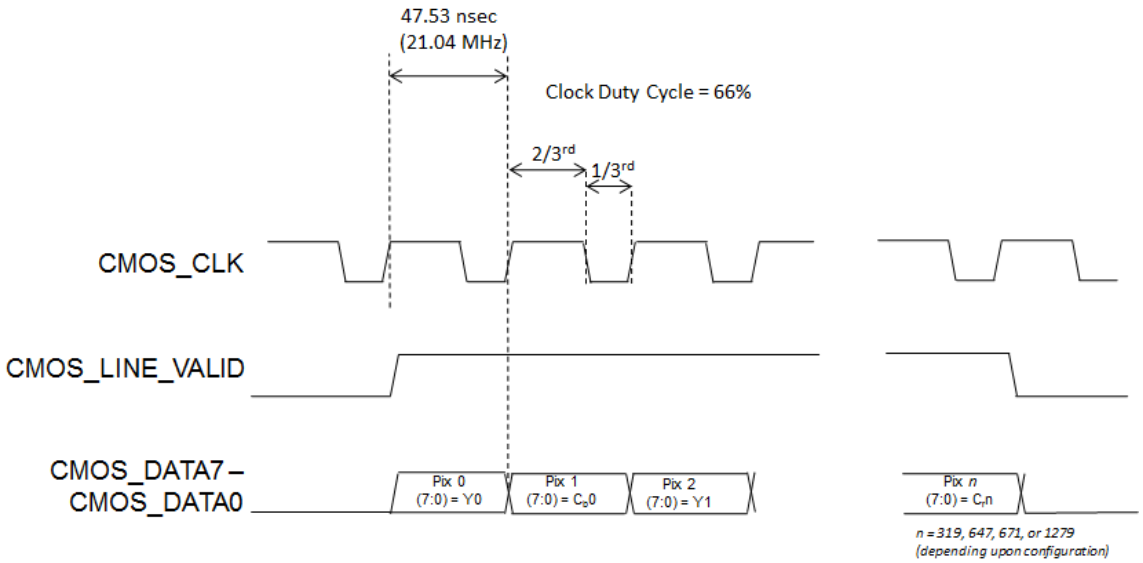
Configuration, Video Speed	Configuration, Resolution	Video Setting	Averager Mode	Frame Rate (Hz)	Frame Rate (Hz) 8-bit Digital eZoom Mode
Fast	324 /336	NTSC	Disabled	59.94 Hz	29.97 Hz
Fast	324 /336	PAL	Disabled	50.00 Hz	25.00 Hz
Fast	324 /336	NTSC	Enabled	29.97 Hz	29.97 Hz
Fast	324 /336	PAL	Enabled	25.00 Hz	25.00 Hz
Fast	640, 30Hz	NTSC	not applicable	29.97 Hz	29.97 Hz
Fast	640, 30Hz	PAL	not applicable	25.00 Hz	25.00 Hz
Fast	640, 60Hz	NTSC	Disabled	59.94 Hz	59.94 Hz
Fast	640, 60Hz	PAL	Disabled	50.00 Hz	50.00 Hz

Fast	640, 60Hz	NTSC	Enabled	29.97 Hz	59.94 Hz
Fast	640, 60Hz	PAL	Enabled	25.00 Hz	50.00 Hz
Slow	324 /336	NTSC	Disabled	7.49 Hz	29.97 Hz
Slow	324 /336	PAL	Disabled	8.33 Hz	25.00 Hz
Slow	324 /336	NTSC	Enabled	7.49 Hz	29.97 Hz
Slow	324 /336	PAL	Enabled	8.33 Hz	25.00 Hz
Slow	640, 30Hz	NTSC	not applicable	7.49 Hz	29.97 Hz
Slow	640, 30Hz	PAL	not applicable	8.33 Hz	25.00 Hz

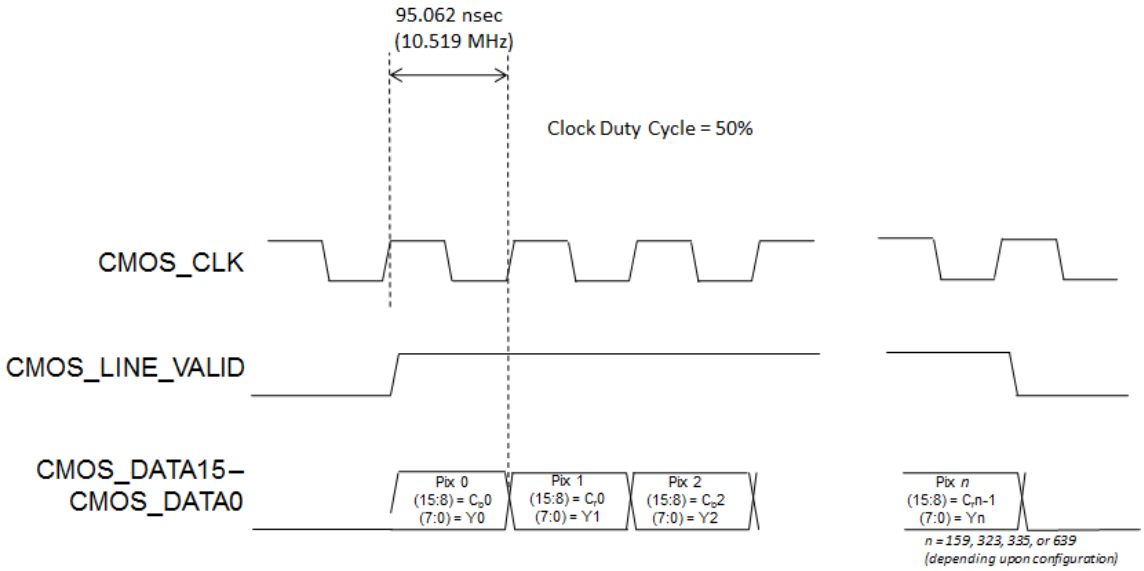
- *Note 1: The resolution value listed in the above table is that shown in the part number of the Tau 2 core. See the Tau 2 Product Specification for further description. It refers to the number of pixel columns.*
- *Note 2: See the Tau 2 Product Specification for a description of the averager feature. The 640 configurations do not provide this feature.*
- *Note 3: The idle time at the end of each frame varies considerably depending upon frame rate and number of pixels per frame.*
- *Note 4: For Tau 2.4 and later releases, the optional "digital eZoom Mode" causes the frame rate to be either 29.97Hz or 25Hz, depending on video setting. For the Tau 2.7 640, 60Hz configuration this rule does not apply. For slow configurations, the frame rate is made up of replicated frames for a true data update rate of only 7.49Hz or 8.33Hz.*
- *Note 5: For Tau 2.4 and later releases, the optional "digital eZoom Mode" also affects the output resolution. The output resolution for the 8-bit CMOS and LVDS channels in this mode will be 640x512 regardless of the native array size.*



(a) 14-bit CMOS Mode



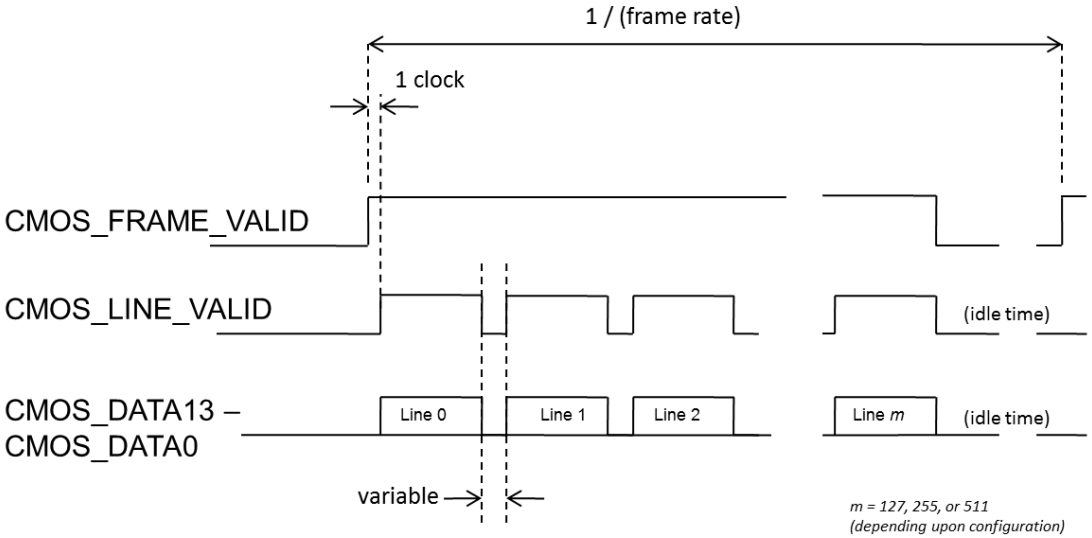
(b) 8-bit Double-Clocked YCbCr CMOS mode ('YCbYCr' 4:2:2 Cosited)



(c) 16-bit YCbCr CMOS mode (4:2:2 Cosited)

Note: Figures are not necessarily to scale

Figure 3: Line Timing, CMOS Protocol



Note: Figure is not to scale.

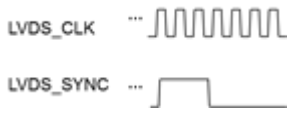
Figure 4: Frame Timing, CMOS Protocol

3.1.4.3 LVDS Protocol

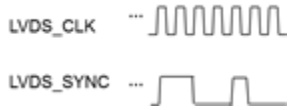
The Tau 2 core provides the option of a digital data protocol used on previous FLIR products including Photon and Tau. Specifically:

1. The channel consists of a clock pair, an encoded sync pair, and two data-line pairs. See Table 1 for pin assignments. All signals employ low-voltage differential signaling (LVDS).
2. The choice between 14-bit (pre-AGC), 8-bit (post-AGC), or 8-bit Bayer colorized, data is field-selectable.
3. The field-selectable choice between 8-bit data with or without the continuous electronic zoom capability is also available. The "digital eZoom Mode" affects frame rate, resolution, and flat-field correction (refer to the Tau 2 Product Specification for further details). In the 8-bit digital eZoom mode with colorization enabled (via the Bayer mode) the user also has the option to enable symbology in the 8-bit channel.
4. The clock rate is 147.27MHz for the 640, 60Hz configuration. The clock rate is 73.636MHz for all other configurations (e.g. 640 30Hz, 336, 324, and 160). One pixel datum is transmitted in each 7-clock period.

   Note: In the original Tau 320 configuration, only a single data line was employed on the LVDS interface. For Tau 2, all configurations utilize two data lines regardless of number of pixels.
5. One sync datum is also transmitted in each 7-clock period. There are three possible 7-bit output values of the sync datum when the LVDS channel is active:
   a. Frame start: 1110000, as depicted in Figure 5a. The frame-sync datum is transmitted 4 pixel periods prior to the start of the first pixel of the first line.
   b. Line valid: 1100100, as depicted in Figure 5b. The line-valid datum is transmitted coincident with each valid pixel on the data lines.
   c. Data invalid: 1100000, as depicted in Figure 5c. The data-invalid datum is transmitted whenever there is no valid data on the data lines.
6. Line timing and sync encoding are shown in Figure 5d. Note that the idle portion of each line varies by configuration but is constant per line. That is, each line spans the same number of clock periods.
7. Phasing of the clock relative to the sync and data signals is shown in Figure 6.
8. The frame rate is identical to that of the CMOS channel as shown in Table 8.
9. No data is output on the LVDS channel during each FFC period. That is, LVDS_SYNC, and LVDS_DATA are both disabled throughout FFC. For Tau 2.4 and later releases, while the "digital eZoom Mode" is selected, the 8-bit data output continues during FFC. That is, the last frame before FFC is replicated during each FFC period. This mode does not affect the 14-bit data output.

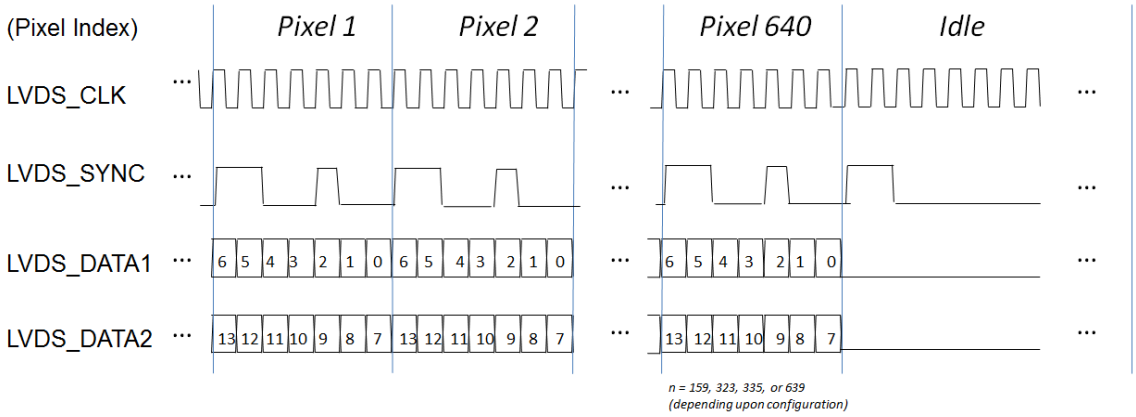


(a) LVDS_SYNC signaling frame start



(b) LVDS_SYNC signaling line valid

(c) LVDS_SYNC signaling data invalid



(d) LVDS Line Timing

Figure 5: Digital Data Timing, LVDS Protocol, all Tau 2 Configurations

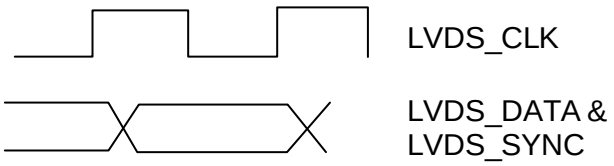


Figure 6: Digital Data Timing, LVDS Clock relative to Data and Sync

3.1.5 Configurable Discrete I/O Pins

Depending upon the XP bus mode (see Table 2), the Tau 2 core provides up to 8 signals referred to as discrete I/O pins (DISCRETE0 – DISCRETE7) that can each be field-configured to provide a specified functionality when shorted to DGND. For example, one of the pins might be configured to toggle between white hot and black hot polarity. The full list of functions that can be assigned to these pins is defined in the Tau 2 Product Specification. There is no de-bounce circuitry on the signals. They are polled at 30Hz.

3.1.6 Frame Synchronization Interface

The Tau 2 core provides the option of transmitting or receiving a frame-synchronization pulse on EXT_SYNC. This feature provides the capability to synchronize frame start between two cores, one configured as master and the other configured as slave, or to synchronize the Tau 2 core with a different camera.

3.1.6.1 Master Mode

When configured as a master, the core transmits a pulse on the frame-synchronization interface at a rate of once per frame. The frame rate is dependent on the video standard (29.97/59.94Hz for NTSC or 25/50Hz for PAL) and for the Tau 2.7 release and later, is also dependent on the averager feature applicable for all configurations except the 640, 30Hz configuration. The frame rate is 59.94/50Hz with the averager disabled and 29.97/25.00Hz with the averager enabled for NTSC and PAL respectively. The pulse complies with the characteristics defined in Table 9.

Table 9: Sync Pulse Characteristics

Mode	Signal Direction	Voltage (relative to DGND)	Frequency Range	Pulse width (minimum)
Master	Output	3.3V	29.97/59.94Hz NTSC, 25.00/50Hz PAL	1 µsec
Slave NTSC, 30Hz (avg enabled)*	Input	3.3V	24.98Hz to 29.98Hz	100 nsec
Slave PAL, 25Hz (avg enabled)*	Input	3.3V	22.25Hz to 27.25Hz	100 nsec
Slave NTSC, 60Hz (avg disabled)*	Input	3.3V	54.94Hz to 59.94Hz	100 nsec
Slave PAL, 50Hz (avg disabled)*	Input	3.3V	47.25Hz to 52.25Hz	100 nsec
Disabled	n/a	3.3V	n/a	n/a

**Note: The 640, 30Hz configuration supports only 30Hz/25Hz modes.*

3.1.6.2 Slave Mode

When configured as a slave, the core synchronizes the FPA frame start to the rising edge of a pulse received on the frame-synchronization interface. The required frequency and pulse width are defined in Table 9; the frequency input is dependent on the configuration of the camera regarding video standard (NTSC/PAL) and averager (enabled/disabled) settings. If the camera is configured as NTSC with averager enabled (or simply NTSC for the 640, 30Hz configuration), any pulses sent at a rate greater than 30Hz will be ignored. (For example, if pulses are sent at 40 Hz (25 msec period), the pulse sent 25 msec after the first will be ignored. The next frame will be triggered on the next pulse for an effective frame rate of 20 Hz.) When in slave mode, the core will not output data until a valid pulse is received. Operating at a frequency different from those specified for each configuration in the table is not recommended due to degradation in image quality.

Note 1: Slave mode is not recommended for synchronizing analog video; this feature is intended for digital video synchronization. For a core configured as a slave, analog video output requires that the pulse timing be sent at a rate confirming to the selected video standard (either NTSC or PAL).

Note 2: The LVDS / CMOS frame sync signals are delayed relative to the External-Frame-Sync pulse. Consequently, digital frame acquisitions should use the appropriate sync signal and not rely on the External Frame Sync pulse for synchronization.

For slow configurations, the output frame rate is a fraction of the sync pulse rate. Because there is ambiguity as to which received pulse triggers the frame timing, FLIR does not recommended to use the external sync interface with a slow-configured Tau 2 core.

3.1.7 Communication Channel

The Tau 2 core provides an asynchronous serial interface consisting of the signals named RS232_RX (input to core), RS232_TX (output from core), and DGND. The interface complies with the RS232 standard except in voltage levels: Full RS-232 levels may be applied to the input, but 3.3V CMOS signal levels are output. The Tau 2 core automatically detects the polarity of incoming messages (standard logic or inverted logic) and replies at the same polarity. The Tau 2 is capable of communication at various baud rates, as further described in the Tau 2 Software IDD. The communication protocol of the RS232 channel is also defined in the Tau 2 Software IDD.

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Contact your nearest FLIR Commercial Systems, Inc. representative for instructions on how to return the product to FLIR for proper disposal.

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